CLAIMS

We claim:

1. A semiconductor structure, comprising:

a first substrate;

a second substrate joined to the first substrate;

a plurality of contacts between the first substrate and the second substrate; and

a plurality of first solder bumps connected between the first substrate and the second substrate for aligning the contacts.

2. The semiconductor structure according to claim 1, wherein the contacts have a different composition than the first solder bumps.

3. The semiconductor structure according to claim 1, wherein at least one of the first substrate and the second substrate is an integrated circuit chip.

4. The semiconductor structure according to claim 1, wherein the contacts comprise second solder bumps.

5. The semiconductor structure according to claim 4, wherein the second solder bumps have a smaller size than the first solder bumps.

6. The semiconductor structure according to claim 1, wherein the contacts have a smaller size than the first solder bumps.

7. The semiconductor structure according to claim 1, wherein the contacts comprise electrically conductive epoxy.

8. The semiconductor structure according to claim 1, wherein the contacts comprise a polymer-metal composite.

9. The semiconductor structure according to claim 1, wherein the contacts comprise at least one member selected from the group consisting of dendrites and self-interlocking micro connectors.

10. The semiconductor structure according to claim 1, wherein the contacts each have a diameter of less than about 50 μm.

11. The semiconductor structure according to claim 1,

wherein the contacts each have a diameter of about 10 μm.

12. The semiconductor structure according to claim 1, wherein the contacts each have a diameter of less than about 10 μm.

13. The semiconductor structure according to claim 1, wherein the contacts have a pitch of less than about 100 μm.

14. The semiconductor structure according to claim 1, wherein the contacts have a pitch of about 30 μm.

15. The semiconductor structure according to claim 1, wherein the contacts have a diameter about 20% of the diameter of the first solder bumps.

16. The semiconductor structure according to claim 1, wherein the contacts comprise a material having a higher melting point that the first solder bumps.

17. The semiconductor structure according to claim 1, wherein an upper surface of the contacts and an upper surface of the first solder bumps are co-planar.

18. The semiconductor structure according to claim 1, further comprising:

a ledge on at least one of the first substrate and the second substrate, wherein the first solder bumps are arranged in contact with the ledge, such that an upper surface of the contacts and an upper surface of the first solder bumps are co-planar.

19. The semiconductor structure according to claim 1, wherein the contacts comprise a material other than solder.

20. The semiconductor structure according to claim 1, wherein the contacts comprise solder.

21. The semiconductor structure according to claim 1, wherein the contacts comprise PMC.

22. The semiconductor structure according to claim 1, wherein the contacts provide optical communication between the first substrate and the second substrate.

23. The semiconductor structure according to claim 1, wherein the contacts comprise a waveguide.

24. The semiconductor structure according to claim 1, wherein the contacts comprise an optical transmitter and an optical receiver.

25. The semiconductor structure according to claim 1, wherein at least one of the first substrate and the second substrate is an integrated circuit chip, and the contacts are sufficiently small to permit alignment of individual devices on the integrated circuit chips.

26. A method of fabricating a semiconductor structure, the method comprising:

providing a first substrate and a second substrate;

providing contacts on one of the first substrate and the second substrate;

providing first solder bumps on one of the first substrate and the second substrate;

mounting the first substrate on the second substrate; and

reflowing the first solder bumps for surface tension aligning of the contacts.

27. The method according to claim 26, wherein the contacts have a different composition than the first solder

bumps.

28. The method according to claim 26, wherein at least one of the first substrate and the second substrate is an integrated circuit chip.

29. The method according to claim 26, wherein the contacts comprise second solder bumps.

30. The method according to claim 29, further comprising:

reflowing the second solder bumps, wherein the second solder bumps ball up to make contact between the first substrate and the second substrate.

31. The method according to claim 29, wherein the second solder bumps comprise a material having a higher melting point that the first solder bumps, and reflowing the second solder bumps requires heating the second solder bumps to a higher temperature than reflowing the first solder bumps.

32. The method according to claim 29, wherein the second solder bumps are provided with a smaller size than

the first solder bumps.

33. The method according to claim 26, wherein the contacts comprise electrically conductive epoxy.

34. The method according to claim 26, wherein the contacts comprise a polymer-metal composite.

35. The method according to claim 26, wherein reflowing the first solder bumps draws the first substrate toward the second substrate to cause the contacts to make contact with the first substrate and the second substrate.

36. The method according to claim 26, wherein the first solder bumps contact the first substrate and the second substrate prior to the contacts making contact between the first substrate and the second substrate.

37. The method according to claim 26, wherein the contacts are provided by thin film processing.

38. The method according to claim 37, wherein the thin film processing comprises lift off stencil or subtractive etch.

39. The method according to claim 26, wherein the contacts each are provided with a diameter of less than about 50 μm.

40. The method according to claim 26, wherein the contacts each are provided with a diameter of about 10 μm.

41. The method according to claim 26, wherein the contacts each are provided with a diameter of less than about 10 μm.

42. The method according to claim 26, wherein the contacts are provided with a pitch of less than about 100 μm.

43. The method according to claim 26, wherein the contacts are provided with a pitch of about 30 μm.

44. The method according to claim 26, wherein the contacts are provided with a diameter about 20 % of the diameter of the first solder bumps.

45. The method according to claim 26, wherein the contacts are provided with a smaller size than the first

solder bumps.

46. The method according to claim 26, wherein the contacts provide optical communication between the first substrate and the second substrate.

47. The method according to claim 26, wherein the contacts comprise a waveguide.

48. The method according to claim 26, wherein the contacts comprise an optical transmitter and an optical receiver.

49. The method according to claim 26, wherein the contacts comprise at least one member selected from the group consisting of dendrites and self-interlocking micro connectors.

50. The method according to claim 26, wherein the contacts and the first solder bumps are provided such that an upper surface of the contacts and an upper surface of the first solder bumps are co-planar.

51. The method according to claim 26, wherein the

contacts comprise at least one member selected from the group consisting of solder, a material other than solder, and PMC.

52. The method according to claim 26, further comprising:

providing a ledge on at least one of the first substrate and the second substrate, wherein the first solder bumps are arranged in contact with the ledge, such that an upper surface of the contacts and an upper surface of the first solder bumps are co-planar.

53. The method according to claim 26, wherein the contacts are compressed as the first solder bumps are reflowed.

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